IN THE CLAIMS

Please amend claim 1.

Please cancel claims 7,10 and 11.

Listing of Claims

1. (currently amended) A method of forming a stress relaxed shallow trench isolation (STI) structure to improve charge mobility of a MOSFET device comprising the steps of:

providing a semiconductor substrate;

forming a trench in the semiconductor substrate;

forming a plurality of liner layers comprising an uppermost plurality of nitride liners selected from the group consisting of silicon nitride (SiN) and silicon oxynitride (SiON) to line the trench;

then forming a plurality of trench filling oxide layers, said plurality of trench filing oxide layers is ~~selected from the group consisting of~~ a spin-on glass (SOG) that ~~and undoped silicate glass (USG); the SOG~~ comprises a precursor selected from the group consisting of organic and inorganic mixtures for forming cross-linked silicon oxide containing structures;

wherein at least one stress relaxing thermal annealing step is carried out during and following formation of said plurality of trench filling oxide layers to form a trench filling substantially free of stress; and,

removing excess trench filling oxide layers above the trench level.

2. (original) The method of claim 1, further comprising forming at least one patterned hardmask layer selected from the group consisting of silicon nitride and silicon oxynitride over said substrate.

3. (original) The method of claim 1, wherein the semiconductor substrate comprises material selected from the group consisting of silicon, silicon germanium, and gallium arsenide.

4. (previously presented) The method of claim 1, wherein the plurality of liner layers comprises a lowermost silicon oxide liner formed according to a method selected from the group consisting of thermal oxidation, LPCVD, and ALCVD.

5. (cancelled)

6. (previously presented) The method of claim 1, wherein the step of forming the uppermost plurality of nitride liners comprises a process selected from the group consisting of treating and underlying thermal oxide liner with nitrogen, and depositing according to a CVD process.

7. (cancelled)

8. (cancelled)

9. (previously presented) The method of claim 1, wherein the precursor comprises a material selected from the group consisting of siloxanes, silanes, and polysesilquioxanes.

10. (cancelled)

11. (cancelled)

12. (previously presented) The method of claim 1, wherein the at least one stress relaxing thermal annealing step thermal annealing step is carried out following formation of each trench filling material layer to a desired filling level.

13. (previously presented) The method of claim 1, wherein the step of carrying out at least one stress relaxing thermal annealing step is carried out in an ambient selected from the group consisting of O_2 and N_2.

14. (previously presented) The method of claim 1, wherein the step of forming a trench comprises forming a trench comprising sidewalls having an angle with respect to a plane parallel to the substrate major surface of between about 80 degrees and about 89 degrees.

15. (previously presented) The method of claim 1, wherein the step of forming a trench comprises forming a trench comprising rounded top and/or bottom corners.

16. (previously presented) A shallow trench isolation (STI) structure with reduced stress to improve charge mobility comprising:

a semiconductor substrate;

a trench formed through a thickness of the semiconductor substrate;

a plurality of liner layers comprising an uppermost plurality of nitride liners selected from the group consisting of silicon nitride and silicon oxynitride lining the trench; and,

a plurality of trench filling oxide layers on the uppermost plurality of nitride liners comprising an SOG layer and an uppermost USG layer, said plurality of trench filling oxide layers substantially free of stress in a direction substantially parallel or perpendicular to the semiconductor substrate major surface, said SOG layer comprises a precursor selected from the group consisting of siloxanes, silicates, and polysesilquioxanes.

17. (previously presented) The STI structure of claim 16, wherein the trench comprises sidewalls having an angle with respect to a plane parallel to the substrate major surface of between about 80 degrees and about 89 degrees.

18. (previously presented) The STI structure of claim 16 , wherein the trench comprises rounded top and/or bottom corners.

19. (previously presented) The STI structure of claim 16, wherein the plurality of trench filling layers comprise a portion that extends above the semiconductor substrate surface.

20. (previously presented) The STI structure of claim 19, wherein the portion comprises an inward edge portion extending higher above the substrate surface compared to an outward edge portion.

21. (cancelled)

22. (cancelled)

23. (previously presented) The STI structure of claim 16, wherein the plurality of trench filling oxide layers comprises a lowermost SOG layer selected from the group consisting of organic and inorganic SOG layers, and an uppermost USG layer.

24. (previously presented) The STI structure of claim 16 , wherein the plurality of trench filling oxide layers comprises a lowermost USG layer, an intervening SOG layer selected from the group consisting of organic and inorganic SOG layers, and an uppermost USG layer.

25. (previously presented) The STI structure of claim 16, wherein the plurality of trench filing oxide layers comprises a plurality of USG layers.

26. (previously presented) The STI structure of claim 16, wherein the plurality of trench filling oxide layers comprises a plurality of SOG layers selected from the group consisting of inorganic SOG layers and organic SOG layers.

27. (cancelled)

28. (previously presented) The STI structure of claim 16, wherein the plurality of nitride liners is formed of one of an SiN/SiON and SiON/SiN stack.

29. (previously presented) The STI structure of claim 16, wherein the plurality of nitride liners is formed on a SiO_2 liner layer.

30. (previously presented) The STI structure of claim 16, wherein the plurality of liner layers is formed of a SiO_2/SiN/SiON stack.

31. (previously presented) The STI structure of claim 16, wherein the plurality of nitride liners comprises one of a SiN/SiON and SiON/SiN stack.

32. (previously presented) The method of claim 1, wherein the plurality of nitride liners comprises one of an SiN/SiON and SiON/SiN stack of layers.

33. (cancelled)

34. (cancelled)